MODELLING AND MEASUREMENT OF MICROSTRIP TRANSMISSION LINE STRUCTURES

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ABSTRACT

New techniques have been employed in both the modelling and measurement of microstrip transmission line structures. The modelling employs a dual potential approach using finite element analysis to derive exact bounds to the microstrip characteristics. The measurement uses an 'on-chip' calibration method with microstrip calibration pieces.

THEORY

This paper describes work done on the modelling of microstrip transmission line structures on both alumina and gallium arsenide (GaAs) substrates, and measurements performed on test structures fabricated on alumina. The work employs new techniques in both of these areas. The importance of accurate analysis and measurement of these types of circuits is paramount, as they are important building blocks in microwave integrated circuit design. This is especially true considering the recent increased interest in GaAs monolithic microwave integrated circuits.

The modelling has been based on a dual potential finite element analysis of the microstrip transmission line structure to derive exact upper and lower bounds to the solution. The finite element approach was adopted due to its flexibility when applied to structures where there are large differences in the dimensions of the elements which comprise the structure. In microstrip the inner dimensions may be two orders of magnitude smaller than the bounding dimensions. Now, given a transmission line with metallic conductors (electric walls) and lines of symmetry (magnetic walls), the potential satisfies Laplace's equation within the bounded cross section.

It is well known that a variational expression exists for the line capacitance of a uniform transmission line with applied potential V :-

$$\frac{CV^2}{\varepsilon_o} = \iint_S \kappa |\nabla\phi|^2 dS$$

where ϕ is the potential function within the cross section and κ is the local dielectric permittivity. Discretisation of the potential over an aggregate of finite elements leads to a simple matrix equation (1) whose unknown is a column vector of discrete potential values.

Once the potential distribution has been solved using F.E. techniques, the line capacitance per unit length can be derived. However, by the minimum energy principle, only the exact potential distribution will result in the exact value for the capacitance, i.e. the F.E. solution is always an upper bound to the correct value. By interchanging the electric and magnetic walls we derive the dual structure, and we can again solve the Laplace equation for the dual potential distribution. It has been shown (2) that this leads to a lower bound for the line capacitance. By solving the microstrip structure with and without the dielectric present, for both the dual potential distributions, exact bounds for both the characteristic impedance and the effective dielectric constant of the microstrip line structure can be derived. The important point to note here is that the exact solution must lie between these upper and lower bounds, and that these bounds may be brought closer together by implementing a finer mesh with more elements in the F.E. analysis. So the accuracy of the solution is only limited by the power and memory capacity of the machine employed to do the computation. The absolute magnitude of the error in line capacitance itself is therefore known and the average of the bounds can realistically be assumed to provide an order of magnitude improvement in the accuracy.

The test structures examined in this work were step-impedance lines where there is a change in the width of the microstrip line. The dimensions of the lines on both alumina and GaAs are shown in Fig 1. The upper and lower bound results are given in the table below the figure. From these the bounds of S-parameters were derived by varying the impedance and effective dielectric constant values within their bounds. The chain matrix for each of the three line sections is given below:

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$$\begin{bmatrix} \cos(\beta l) & jZ_o \sin(\beta l) \\ jY_o \sin(\beta l) & \cos(\beta l) \end{bmatrix}$$

where Z_o is the calculated charateristic impedance, $Y_o = 1/Z_o$ and βl is the electrical length of the line (dependent on frequency and the calculated effective dielectric constant). The three chain matrices are cascaded into an overall chain matrix, which is then converted into the S-parameters of the line structure. This structure is symmetrical, ie S11=S22 and S21=S12, so only the S11 and S21 results are quoted here. This process is repeated many times to build up a range of possible S-parameters.

MEASUREMENT

Considering now the measurement technique, the S-parameter measurements were performed using standard automatic network analyser equipment. However, the critical aspect of S-parameter measurement is the calibration routine to apply accuracy enhancement by error correction techniques (3). If this is done using standard co-axial calibration pieces, then further processing of the results is required to remove the effect of the launcher which connects the co-axial test ports to the microstrip structure under test. This requires very accurate modelling of the launcher characteristics which is difficult particularly over broad frequency ranges. To try to overcome this problem, the approach of 'on-chip' calibration is being considered by many workers. In this technique the calibration pieces are formed in the same medium as the circuit under test, and the reference plane of the measurement is on the circuit rather than outside it. A successful technique has been developed using coplanar waveguide calibration pieces (4), but for this work we have developed a technique using microstrip calibration pieces, because we wish to measure microstrip components. The calibration pieces used are a zero length short circuit, open circuits at the ends of lines of known length, and a through line of characteristic impedance of 50Ω. Software has been developed for standard 8- and 12-term error correction, and a series of measurement jigs built to accommodate test substrates of different substrate thicknesses. Measurements have been performed on substrates of both RT-Duroid and alumina.

Fig 2 shows both the modelled and measured results for the alumina step impedance line, including both S11 and S21 magnitude and phase. The results are shown in terms of error bars, the two bars being slightly offset from one another for clarity. The error bar for the modelled results is derived directly from the upper and lower bound results of characteristic impedance and effective dielectric constant. For the measured results it is extremely difficult to derive correct error bars, due to the complex nature of the measurement equipment and the calibration process. The error bars shown are derived from statistical data of the repeatability of several calibration and measurement operations. They are therefore likely to provide optimistic limits.

Fig. 3 shows the modelled results for the GaAs step impedance line, again showing the range of predicted values.

In summary, both theoretical and experimental results have been presented for a microstrip test structure. New approaches have been adopted for both modelling and measurement in an attempt to independently improve the accuracy of both techniques, and so improve the confidence and reliability of design in a vital area of microwave integrated circuit production.

REFERENCES

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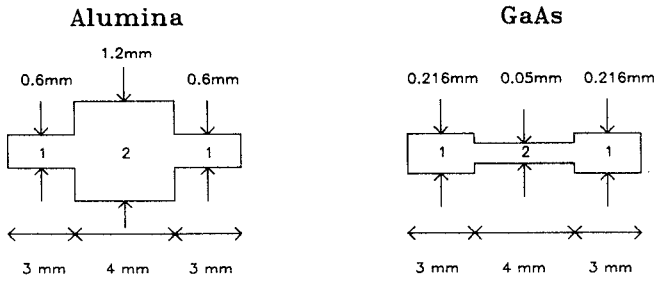
(3) J. Fitzpatrick, 'Error Models for Systems Measurement', Microwave Journal, pp 63-66, May 1978.

(4) E. W. Strid & K. R. Gleason, 'A D.C. - 12 GHz Monolithic GaAs FET Distributed Amplifier', IEEE Trans., Vol. ED-29, No. 7, July 1982.

Fig. 1 Step Impedance Line Test Structure Layout



0.625 mm Substrate

	Upper	Lower	
Impedance (Ohms)	50.46	48.57	①
Eff. Dielect. Const.	6.53	6.49	
Impedance (Ohms)	34.33	33.41	②
Eff. Dielect. Const.	6.95	6.93	

0.3 mm Substrate

	Upper	Lower
Impedance (Ohms)	50.73	49.22
Eff. Dielect. Const.	8.26	8.19
Impedance (Ohms)	83.88	79.82
Eff. Dielect. Const.	7.58	7.55

Fig. 2a S11 Mag. Step Impedance Line on Alumina

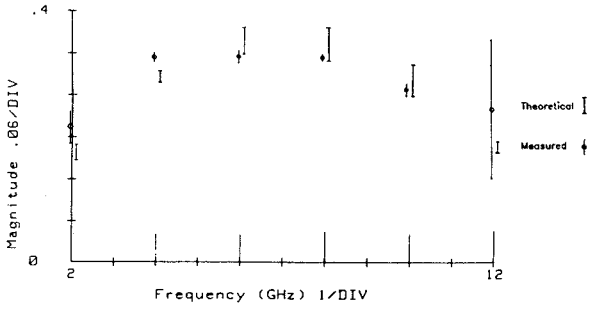


Fig. 2b S11 Phase. Step Impedance Line on Alumina

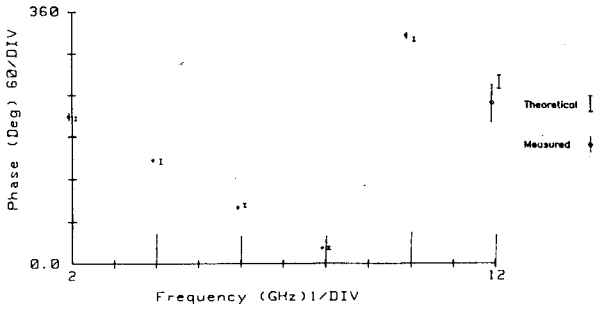


Fig. 2c S21 Mag. Step Impedance Line on Alumina

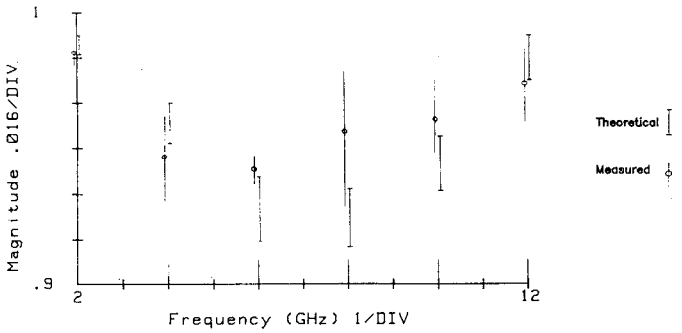


Fig. 2d S21 Phase. Step Impedance Line on Alumina

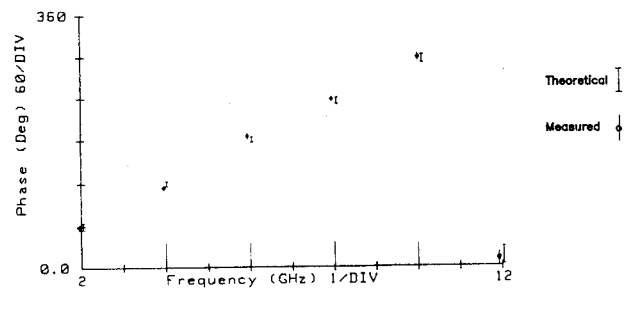
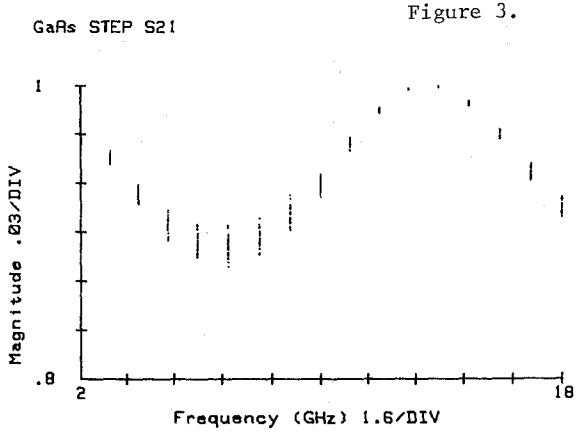
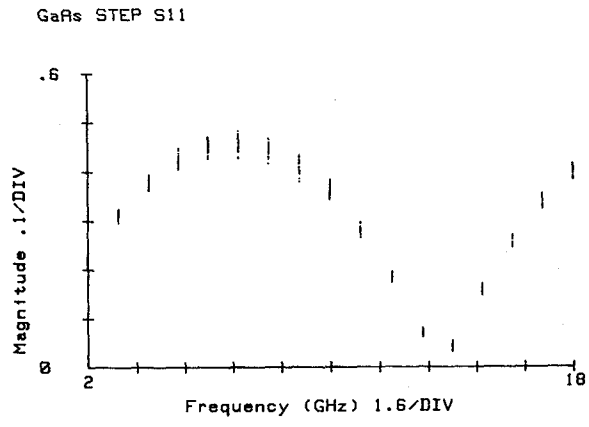
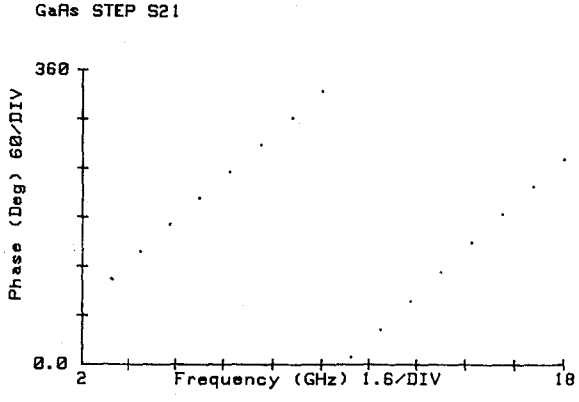
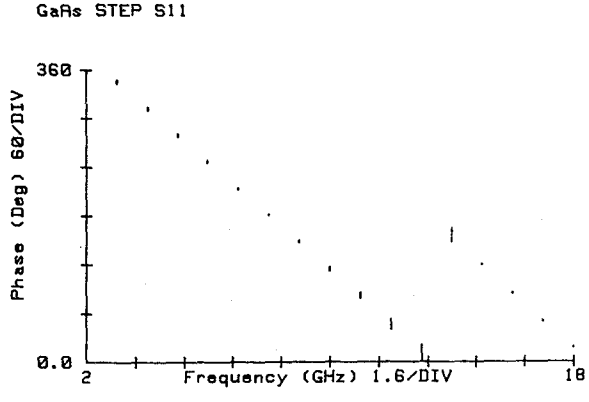


Figure 3.


GaAs STEP S21
1
.8
Magnitude .03/DIV
2
18
Frequency (GHz) 1.6/DIV


GaAs STEP S11
.6
0
Magnitude .1/DIV
2
18
Frequency (GHz) 1.6/DIV


GaAs STEP S21
360
0.0
Phase (Deg) 60/DIV
2
Frequency (GHz) 1.6/DIV
18


GaAs STEP S11
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0.0
Phase (Deg) 60/DIV
2
Frequency (GHz) 1.6/DIV
18